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(54)[TITLE OF THE INVENTION] LIQUID CRYSTAL DISPLAY DEVICE

(57)[Abstract]

[PURPOSE] The present invention aims at providing a liquid crystal display device at an increased production yield with a reduced production cost.

[CONSTITUTION] A liquid crystal display device comprising a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor and a second substrate opposed to the first substrate, and a liquid crystal composition having sandwiched therebetween, wherein at least one part of said peripheral circuits being connected to the matrix wirings in X-direction or Y-direction formed on the first substrate has a complementary structure with active elements to form thin film transistors fabricated by the same process, and the remaining parts of the peripheral circuits are constructed from semiconductor chips.

[WHAT IS CLAIMED IS:]

1. A liquid crystal display device comprising:

a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor established in complementary structure;

a second substrate opposed to the first substrate; and

a liquid crystal composition having sandwiched between the first substrate and the second substrate, wherein, among the peripheral circuits being connected to the matrix wirings in X-direction or Y-direction formed on the first substrate, at least one part of said peripheral

circuits is constructed from thin film semiconductor devices fabricated in complementary structure by the same process utilized for the thin film transistors, and the remaining halves of the peripheral circuits are constructed from semiconductor chips.

2. The liquid crystal display device of claim 1 wherein the peripheral circuits constructed from semiconductor chips is connected to the matrix wirings by COG method.

3. The liquid crystal display device of claim 1 wherein the thin film transistor is constructed from semi-amorphous semiconductor.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF THE INVENTION]

The present invention relates to a liquid crystal display device formed by using thin film transistors.

[0002]

[DESCRIPTION OF PRIOR ART]

More attention is paid to flat displays than to CRTs for use in office automation (OA) machines and the like, and particularly, there is an increasing demand for large-area display devices. Also, as other application of flat displays, wall television (TV) is developed at a fast speed. Furthermore, there are demands for color flat displays and finer display images.

[0003]

A liquid crystal display device is known as a representative example of the flat displays. The liquid crystal display device comprises a liquid crystal composition having an electrode interposed between a pair of glass substrates, and the images are displayed by the change of state of the liquid crystal composition upon application of an electric field thereto. The liquid crystal may be driven by the use of a thin film transistor (referred to hereinafter as a TFT) or other switching elements, or by making it into a simple matrix structure. In any case, a driver circuit is established at the periphery of a display to supply signals for driving liquid crystals to column and row directions (X, Y).

[0004]

The driver circuit is generally composed of MOS integrated circuit (IC) made of a single crystal silicon. The IC is provided with pad electrodes

corresponding to each of the display electrodes, and a printed substrate is incorporated between the pad and the display electrodes to connect first the pad electrode of the IC with the printed substrate and then the printed substrate with the display. The printed substrate is made of an insulator substrate such as a glass epoxy or a paper filled epoxy, or of a flexible plastic substrate. It requires an area equivalent to or even larger than the display area. Similarly, the volume thereof should have to be made considerably large.

[0005]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

Thus, because of the construction as described hereinabove, a conventional display has defects as follows.

[0006]

Namely, (1) a superfine display cannot be realized since the same number of the display electrodes for the X direction and the Y direction of the matrix wirings, or the source (drain) wirings, or the gate wirings should be connected to the printed substrate, and the distance between the connecting portions technologically achievable by the up-to-date surface mounting technology is limited to a certain length.

[0007]

(2) A display device needs the printed substrate, the ICs, and the connecting wirings in addition to the display itself, which require an area and volume about several times as large as those of the display itself.

[0008]

(3) The connections are of low reliability since quite a large number of connections should be established between the main display and the printed substrate, as well as between the printed substrate and the ICs; moreover, not a small weight is casted on the connecting portions.

[0009]

As a means to overcome the foregoing defects, there is a proposal that a display device, particularly a display using active elements as the switching element construct the active element and the peripheral circuits on a same substrate using TFTs. Such a construction indeed solves the three problems mentioned hereinabove, however, it newly develops problems as follows.

[0010]

(4) Since the peripheral circuits as well as an active element also are made from TFTs, the number of the elements to be fabricated on the same substrate is increased and hence the production yield of the TFT is lowered. Therefore, the production yield of the display is decreased.

[0011]

(5) The peripheral circuit portion comprises a very complicated element structure as compared with the element structure at a portion of active elements. Therefore, circuit patterns are complicated and the technique of manufacturing processes became high-level, thereby the production cost is increased. Furthermore, with the increase in the multilayered wiring portion, an increase in process steps as well as a decrease in the production yield of the TFTs occur.

[0012]

(6) Since a quick response is required to the transistors which constitute the peripheral circuit, a polycrystalline semiconductor is generally used. Therefore, it requires a treatment at a high temperature and hence an expensive quartz substrate should be used to obtain a polycrystalline semiconductor layer.

[0013]

[CONSTITUENTS OF THE INVENTION]

The present invention solves the six problems mentioned above by taking balance among them and provides a low-priced liquid crystal display device at a high production yield.

[0014]

Namely, the present invention have been attained by a liquid crystal display device comprising a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor established in a complementary structure and a second substrate opposed to the first substrate, and a liquid crystal composition having sandwiched therebetween, wherein, among the peripheral circuits being connected to the matrix wirings in X-direction or Y-direction, at least one part of said peripheral circuits is established in complementary structure by the same process utilized for the active element connected to the pixel, and the rest of the peripheral circuits are constructed from semiconductor chips.

[0015]

The ICs of the residual peripheral circuits which are not fabricated as TFTs are connected with the substrate by a COG process which comprises directly mounting the IC chips on a substrate and connecting them with each of the connecting terminals, and a TAB process which comprises mounting each of the IC chips on a flexible substrate made of an organic resin, and then connecting the resin substrate with the display substrate.

[0016]

According to the present invention, all of the peripheral circuits are not fabricated as TFTs. In stead of this, only a part having simple element structure, or only a functional portion having a small number of elements, or only a circuit portion which is difficult portion of a general use ICs, or only a portion which has expensive ICs is fabricated as TFTs, thereby production yields of liquid crystal display devices are improved and the production cost are reduced.

[0017]

Also, one part of peripheral circuits is fabricated as TFTs, the manufacturing cost is reduced by decreasing the number of external Ics. Conventionally, quite large number of the external Ics have been required.

[0018]

Further, since the thin film transistor has a complementary structure (CTFT) wherein active elements and the peripheral circuits are fabricated by the same process, the ability of driving the pixels is improved and the peripheral circuits has redundancy, thereby it is possible to drive the liquid crystal display device.

[0019]

If the peripheral circuits were to be wholly fabricated into TFTs, the device requires extension of the display substrate along both of the X and Y directions. This leads to an increase in the total occupancy area of the display device itself. In contrast, if only one part of the peripheral circuits were to be fabricated into TFTs, it results a little extension of the substrate which can be readily accommodated to the outer dimension of the computers and other apparatuses to which the display device is assembled. Thus, there is provided a display device having a small occupancy area and volume.

[0020]

A high-leveled technique is required to fabricate the complicated portions of element structure in the peripheral circuit, for example, a element structure which requires a multilayered wiring, or a portion having a function as an amplifier. However, by fabricating one part into TFTs, the conventional ICs are used in a portion where high technique is required and simple element structure or portions of simple function can be made with TFTs. As a result, a display device can be realized at reduced cost with a high yield.

[0021]

Furthermore, by fabricating only one part into TFTs, the number of the TFTs in the peripheral circuit portion can be considerably reduced. For example, the number of the TFTs can be almost halved in the case that the

peripheral circuits for the X and the Y directions have the same function. In this way, it is possible, by reducing the number of elements to be fabricated as TFTs, to increase the production yield of the substrate. In addition, there is provided a low cost display device reduced both in the area of the substrate and in volume.

[0022]

It is further possible to fabricate the semiconductor layers of the TFTs at a lower temperature and yet to realize quick response TFTs having a considerably increased carrier mobility by using semi-amorphous semiconductor according to a new concept , instead of the conventional polycrystalline or amorphous semiconductors used for TFTs,.

[0023]

The semi-amorphous semiconductor can be obtained by applying a heat treatment to crystallize a thin film having deposited by processes such as low-pressure chemical vapor deposition (LPCVD), sputtering, plasma-assisted chemical vapor deposition (PCVD), and the like. The process for fabricating a semi-amorphous semiconductor film is described below referring to the sputtering process as an example.

[0024]

Namely, sputtering is performed by using a single crystal silicon semiconductor as a target under a mixed gas comprising hydrogen and argon. Then, the heavy argon atoms strike the surface of the silicon target, thereby silicon atoms are released from the target and then travel to the substrate on which the film is to be deposited, accompanied by clusters composed of several tens to several millions of silicon atoms.

[0025]

During their travel, hydrogen atoms come to bond with the dangling bonds of the silicon atoms located at the outer periphery of the clusters, and these clusters comprising the silicon-hydrogen bonding are maintained to the surface of the substrate to deposit as a relatively ordered region. Thus, a highly ordered film comprising a mixture of pure amorphous silicon and clusters accompanied by Si-H bondings on the periphery is realized on the surface of the substrate. By further heat treatment of the deposited film at the temperature range of from 450 to 700°C in a non-oxidizing atmosphere, the Si-H bondings on the outer periphery of the clusters react with each other to yield Si-Si bondings.

[0026]

The Si-Si bondings thus obtained exert a strong attractive force to each other. At the same time, however, the clusters in their highly ordered state

are susceptible to undergo phase transition to attain a more ordered state, i.e., a crystallized state. Thus, because the Si-Si bondings in the neighboring clusters attract each other, the resulting crystals suffer lattice distortion which can be observed by laser Raman spectroscopy as a peak deviated in position to the lower frequency side from the 520cm^{-1} which corresponds to the peak of a single crystal of silicon.

[0027]

Furthermore, since the Si-Si bondings between the neighboring clusters cause anchoring (connecting) effects, the energy band in each cluster is electrically connected with that of the neighboring cluster through the anchored locations. Accordingly, since there is no grain boundaries as in the conventional polycrystalline silicon which function as a barrier to the carriers, a carrier mobility as high as in the range of from 10 to 200cm^2/V.sec can be obtained.

[0028]

That is, the semi-amorphous semiconductor defined above has apparently crystallinity, however, if viewed from the electrical properties, there can be assumed a state substantially free from grain boundaries. If the annealing of a silicon semiconductor were to be effected at a temperature as high as 1000°C or over, instead of a moderate annealing in the temperature range of from 450 to 700°C as referred hereinbefore, the crystallization naturally would induce crystal growth to precipitate oxygen and the like at the grain boundaries and would develop a barrier. The resulting material is then a polycrystalline material comprising single crystals and grain boundaries.

[0029]

In the semi-amorphous semiconductors, the carrier mobility increases with elevating degree of anchoring. To enhance the carrier mobility, the oxygen content of the film should be controlled to 7 X 10^{19} cm^{-3} or lower, preferably, to 1 X 10^{19} cm^{-3} or lower, thereby the crystallization can be taken place at a temperature lower than 600°C and high carrier mobility can be obtained.

[0030]

[EXAMPLE 1]

In the present example, a liquid crystal display device having an m X n circuit structure shown in FIG. 1 is described. Namely, among peripheral circuits being connected to a wiring of the X-direction shown in Fig. 1, only analog switch alley circuit portion 1 is fabricated as TFTs 5 in a similar manner as an active element provided to a pixel 6. Also, only analog switch

array portion 2 in the peripheral portion connected to wirings in Y-direction is fabricated in TFTs and the residual peripheral circuit portions connected to substrates as IC4 by COG method. According to the present invention, the peripheral circuit portion fabricated as TFTs is formed as a CTFT in a similar manner as an active element provided in pixels.

[0031]

The actual arrangement of the electrodes and the like corresponding to this circuit structure is shown in FIG. 2. In FIG. 2, however, the structure is simplified and shown in a 2 X 2 structure.

[0032]

Referring to FIG. 3, the process for fabricating the TFTs of the liquid crystal display device according to the present invention is firstly explained. In FIG. 3(A), a silicon oxide film is deposited to a thickness of from 1,000 to 3,000Å as a blocking layer 51 by magnetron radio frequency (RF) sputtering on a glass substrate 50 made of an economical glass such as a quartz glass which resists to heat treatment performed at a temperature of 700°C or less, e.g., about 600°C. The actual film deposition was carried out in a 100% oxygen atmosphere at a film deposition temperature of 15°C, at an output of from 400 to 800W, and a pressure of 0.5 Pa. The film deposition rate using a quartz or a single crystal silicon as the target was in the range of from 30 to 100Å/minute.

[0033]

On the silicon oxide film thus obtained was further deposited a silicon film by LPCVD (low-pressure chemical vapor deposition), sputtering, or plasma-assisted CVD (PCVD). In the case of using the LPCVD process, film deposition was conducted at a temperature lower than the crystallization temperature by 100 to 200°C, i.e., in the range of from 450 to 550°C, e.g., at 530°C, by supplying disilane (Si_2H_6) or trisilane (Si_3H_8) to the CVD apparatus. The pressure inside the reaction chamber was controlled to be in the range of from 30 to 300 Pa. The film deposition rate was 50 to 250Å/minute. Furthermore, optionally boron may be supplied to 1 X 10^{15} to 1 X 10^{18} cm^{-3} in the film as diborane during the film deposition to control the threshold voltage (Vth) of the N-TFT and that of the P-TFT to be approximately the same.

[0034]

In the case of using sputtering, the back pressure prior to sputtering was controlled to 1 X 10^{-5} Pa or lower and film deposition was conducted using a single crystal silicon as the target in an atmosphere having an argon added with hydrogen of 20 to 80%. For example, the atmosphere contains

20% of argon and 80% of hydrogen. The film was deposited at a film deposition temperature of 150°C, a frequency of 13.56 MHz, a sputter output of from 400 to 800W, and a pressure of 0.5 Pa.

[0035]

In the case of depositing a silicon film by a plasma CVD process, the temperature was maintained, e.g., at 300°C, and monosilane (SiH_4) or disilane (Si_2H_6) was used. A high frequency electric power was applied at 13.56 MHz to the gas inside the PCVD apparatus to effect the film deposition.

[0036]

The films thus obtained by the foregoing processes preferably contain oxygen at a concentration of 5×10^{21} cm^{-3} or lower. If the oxygen concentration is too high, the film thus obtained would not crystallize. Accordingly, there would be required to elevate the thermal annealing temperature or to take a longer time for the thermal annealing. Too low an oxygen concentration, on the other hand, increases an off-state leak current due to a backlighting. Accordingly, the preferred range of the oxygen concentration was set in the range of from 4×10^{19} to 4×10^{21} cm^{-3}. The hydrogen concentration was for example 4×10^{20} cm^{-3}, which accounts for 1% by atomic with respect to the silicon concentration of 4×10^{22} $atoms.cm^{-3}$ To enhance crystallization of the source and drain portions, oxygen concentration is 7×10^{19} cm^{-3} or less, preferably 1×10^{19} cm^{-3} or less and oxygen may be added selectively by ion-implantation to the channel forming regions of the TFT which constitute the pixel, to such an amount to give a concentration in the range of from 5×10^{20} to 5×10^{21} cm^{-3}. Since no light was irradiated to the TFTs in the peripheral circuit, it was effective to impart thereto a higher carrier mobility while reducing the oxygen concentration in order to realize a high frequency operation.

[0037]

After the amorphous silicon film was deposited at a thickness of from 500 to 5,000Å, e.g., at a thickness of 1,500Å, the amorphous silicon film was then heat-treated at a moderate temperature in the range of from 450 to 700°C for a duration of from 12 to 70 hours in a non-oxidizing atmosphere. More specifically, the film was maintained at 600°C under a hydrogen atmosphere. Since on the surface of the substrate was provided an amorphous silicon oxide layer under the silicon film, the whole structure was uniformly annealed because there was no nucleus present during the heat treatment. That is, during the film deposition step, the film construction maintains the amorphous structure and the hydrogen is present as a mixture.

[0038]

The silicon film then undergoes phase transition from the amorphous structure to a structure having a higher degree of ordering by the annealing, and partly develops a crystallized portion. Particularly, the region which attains a relatively high degree of ordering at the film deposition of silicon tend to crystallize at this stage. However, the silicon bonding which bonds the silicon atoms each other attracts a region to another. This effect can be observed by a laser Raman spectroscopy as a peak shifted to a lower frequency side as compared with the peak at 522cm^{-1} for a single crystal silicon. The apparent grain size can be calculated by the half width as 50 to 500Å, i.e., a size corresponding to that of a microcrystal, but in fact, the film has a semi-amorphous structure comprising a plurality of those highly crystalline regions yielding a cluster structure, and the clusters are anchored to each other by the bonding between the silicon atoms.

[0039]

As a result, the film yields a state in which no grain boundary (referred to hereinafter as GB) exists. Since the carrier easily moves between the clusters via the anchoring, a carrier mobility far higher than that of a polycrystalline silicon having a distinct GB can be realized. More specifically, a hole mobility(μh) in the range of from 10 to 200cm^2/Vsec and an electron mobility (μe) in the range of from 15 to 300cm^2/Vsec are achieved.

[0040]

On the other hand, if a high temperature annealing in the temperature range of from 900 to 1200°C were to be applied in the place of a moderate temperature annealing as described hereinabove, impurities undergo a solid phase growth from the nuclei and segregate in the film. This results in the high concentration of oxygen, carbon, nitrogen, and other impurities at the GB into a barrier. Thus, despite the high mobility within a single crystal, the carrier is interfered at its transfer from a crystal to another by the barrier at the GB. In practice, it is quite difficult to attain a mobility higher than or equal to 10cm^2/Vsec with a polycrystalline silicon at the present. Thus, in the example, a semi-amorphous or a semi-crystalline structured silicon semiconductor is utilized.

[0041]

Referring to FIG. 3(A), the silicon film was masked with a first photomask <l>, and subjected to photo-etching to obtain the region 22 (having a channel width of 20μm) for the P-TFT on the right-hand side of the FIGURE and the region 13 for the N-TFT on the left-hand side of the FIGURE.

[0042]

On the resulting structure was deposited a silicon oxide film as the gate insulating film to a thickness of from 500 to 2,000Å, e.g., 1,000Å. The conditions of the film deposition were the same as those employed in depositing the silicon oxide film as a blocking layer. Alternatively, a small amount of fluorine may be added during the film deposition to fix sodium ions.

[0043]

Further on the gate insulating film was deposited a silicon film doped with phosphorus at a concentration of from 1 X 10^{21} to 5 X 10^{21} cm^{-3}, or a multilayered film composed of said silicon film doped with phosphorus, having provided thereon a layer of molybdenum (Mo), tungsten (W), $MoSi_2$, or WSi_2. The resulting film was patterned using a second photomask <2> to obtain a structure as shown in FIG. 3(B). Then, a gate electrode 55 for the P-TFT, and a gate electrode 56 for the NTFT were established, for example, by depositing first a 0.2μm thick phosphorus(P)-doped silicon and a 0.3μm thick molybdenum layer thereon, at a channel length of 10μm. Referring to FIG. 3(C), a photoresist 57 was provided using a photomask <3>, and to a source 59 and a drain 58 for the P-TFT were added boron by ion implantation at a dose of from 1 X 10^{15} to 5 X 10^{15} cm^{-2}. Then, as shown in FIG. 3(D), a photoresist 61 was provided using a photomask <4>, and to a source 64 and a drain 62 for the N-TFT was added phosphorus by ion implantation at a dose of from 1 X 10^{15} to 5 X $10^{15}cm^{-2}$.

[0044]

The processes above were carried out via a gate insulating film 54. However, referring to FIG. 3(B), the silicon oxide on the silicon film may be removed utilizing the gate electrodes 55 and 56 as the masks, and then boron and phosphorus may be directly added to the silicon film by ion implantation.

[0045]

The structure thus obtained was re-annealed by heating at 600°C for a duration of from 10 to 50 hours. The impurities in the source 59 and drain 58 of the P-TFT and those in the source 64 and drain 62 of the N-TFT were activated to obtain P^+ and N^+ TFTs. Under the gate electrodes 55 and 56 were provided channel forming regions 60 and 63 with a semi-amorphous semiconductor.

[0046]

According to the process, a CTFT can be obtained in a self-aligned method without elevating the temperature to 700°C or higher. Thus, there is no need to use a substrate made of an expensive material such as quartz, and

therefore it can be seen that the process is suited for fabricating liquid crystal display devices of large pixels according to the present invention.

[0047]

The thermal annealing in this example was conducted twice, i.e., in the steps of fabricating the structures shown in FIGS. 3(A) and 3(D). However, the annealing at the step illustrated in FIG. 3(A) may be omitted depending on the desired characteristics, and the annealing at the step shown in FIG. 3(D) can cover the total annealing. In this way it is possible to speed up the fabrication process. Referring to FIG. 3(E), a silicon oxide film was deposited as an interlayer insulator 65 by the sputtering process mentioned hereinbefore. The method of depositing the silicon oxide film is not restricted to a sputtering method, and there may be employed LPCVD, photo CVD, or normal pressure CVD. The silicon oxide film was deposited, e.g., to a thickness of from 0.2 to 0.6μm, and an opening 66 for the electrode is formed by using a photomask <5>. The structure was then wholly covered with aluminum by sputtering, and after providing lead portions 71 and 72, as well as contacts 67 and 68 using a photomask <6>, the surface thereof was coated with a smoothing film of an organic resin 69 such as a transparent polyimide resin, and subjected again to perforation for the electrodes using a photomask <7>.

[0048]

As shown in FIG. 3(F), two TFTs were established in a complementary structure. To the output terminal thereof was provided an Indium Tin Oxide (ITO) film by sputtering to thereby connect the TFTs with one of the transparent pixel electrodes of the liquid crystal display device. In this case, the ITO film was deposited in the temperature range from room temperature to 150°C, and then finished by annealing in oxygen or in atmosphere in the temperature range of from 200 to 400°C. The ITO film was then etched using a photomask <8> to form an electrode 70. Thus was finally obtained a structure comprising a P-TFT 22, an N-TFT 13, and an electrode 70 made of a transparent conductive film on a single glass substrate 50. The resulting TFT yielded a mobility of 20 (cm^2/Vs) and a Vth of -5.9 V for the P-TFT, and a mobility of 40(cm^2/Vs) and a Vth of 5.0 V for the N-TFT.

[0049]

Referring to FIG. 2, the arrangement of electrodes and the like in the pixel portion of the liquid crystal display device is explained. An N-TFT 13 is assembled at the crossing of a first scanning line 15 and a data line 21, and another pixel N-TFT is provided at the crossing of the first scanning line 15 with another data line 14. On the other hand, a P-TFT is assembled at the

crossing of a second scanning line 18 and a data line 21. Further, to the neighboring crossing of another first scanning line 16 and the data line 21 is provided another pixel N-TFT. Thus is accomplished a matrix structure using CTFTs. The N-TFT 13 is connected to the first scanning line 15 via a contact at the input terminal of the drain portion 64, and the gate portion 56 is connected to the data line 21 established in a multilayered wiring structure. The output terminal of the source portion 62 is connected to the pixel electrode 17 via a contact.

[0050]

The P-TFT 22, on the other hand, is connected to the second scanning line 18 by the input terminal of the drain portion 58 via a contact, while the gate portion 55 is connected to the data line 21, and the output terminal of the source portion 59 is connected to the pixel electrode 17 via a contact in the same manner as in the N-TFT. In this manner, a single pixel is established between (inner side) a pair of scanning lines 15 and 18, with a pixel 23 comprising a transparent conductive film and a CTFT. By extending this basic pixel structure in four directions, a 2 X 2 matrix can be scaled up to give a large pixel liquid crystal display device comprising a 640 X 480 or a 1280 X 960 matrix.

[0051]

It can be seen therefrom that the peripheral circuit is provided as a CMOS structure comprising an N-TFT 13 and a P-TFT 22 both fabricated in the same process as that employed for the switching element.

[0052]

As mentioned above, the substrate was laminated with the facing substrate by a known process, and an STN (super-twisted nematic) liquid crystal was injected between the substrates. The ICs 4 were used for the residual peripheral circuit. The ICs 4 were connected with each of the wirings for the X direction or Y direction on the substrate by a COG process. The ICs 4 are respectively connected to power source and connection lead for supplying data, however, all of one surface substrate is not covered with EPC for connection. Therefore, the number of the connecting portion is considerably decreased and the reliability is improved. As mentioned above, the liquid crystal display device according to the present invention is completed.

[0053]

In the embodiment, only analog switching array portion 1 among the peripheral circuits at the side of the X-direction was fabricated as TFTs and only analog switching array portion 2 among the peripheral circuits at the

side of the Y-direction was fabricated as TFTs. C/TFT is fabricated in a similar process as a switching element while the rest of the peripheral circuits are constructed as ICs 4. The present invention, however, is not only limited to this construction, and the portion which can be more easily fabricated into TFTs can be selected depending on the yield and the problems related to the process technology at the fabrication of the TFTs.

[0054]

As described above, semi-amorphous semiconductor was used as a semiconductor film and it yields a mobility ten times as high as, or even higher than that of the TFT using a conventional non-single crystal semiconductor. Thus, it can be applicable for the TFT in the peripheral circuits in which a rapid response is required, without subjecting the TFTs in the peripheral circuit portion to a special crystallization treatment which was requisite in the conventional TFTs; as a result, the TFTs for the peripheral circuit portion could be fabricated by the same process utilized for fabricating an active element.

[0055]

Also, since an active element connected to the pixels in a liquid crystal is fabricated in C/TFT structure, the operational margin is increased and the electric potential of pixels is stable to keep a certain display level. Also, if one of TFTs is defective, it has an advantage that there is no remarkable defect in display.

[0056]

[EXAMPLE 2]

In FIG. 4 is given a schematic view of a liquid crystal display device according to another embodiment of the present invention. The basic circuits and the like are the same as those employed in the liquid crystal display device described in Example 1. Referring to FIG. 4, the portions constructed with ICs 4 among the peripheral circuits connected to the wirings for the Y-direction have the IC directly provided on the substrate by a COG method.

[0057]

The pad electrodes of the ICs 4 can be connected with the wirings of the Y-direction at a narrower interval instead of the case of forming ICs at only one side. Thus, the process of the present example enables a finer display pixel design. Furthermore, since the ICs are provided on the substrate, the total volume of the display device remains almost unchanged to give a thinner liquid crystal display device.

[0058]

In the examples described above, the TFTs of the active element were

each fabricated into a CMOS structure. However, this structure is not limited to the structure but the structure with only N-TFTs or with only P-TFTs are also acceptable. In the case, however, the number of the elements in the peripheral circuit would be increased.

[0059]

Furthermore, the position at which the TFTs are established can be varied. That is, the TFT need not be provided only to one side, i.e., only to either of the sides connected to the wirings of the X direction and the Y direction, but there may be also provided a second TFT on the other side to connect the TFTs in turns to halve the TFT density. Such a structure realizes an increase in the production yield.

[0060]

[EFFECTS OF THE INVENTION]

According to the present invention, the superfine liquid crystal display devices can be realized with no limitations of the outer connection. Furthermore, the reliability on the connections is improved, since unnecessary connections between the outer peripheral circuits and the wirings along the X and Y directions are minimized.

[0061]

The area occupation of the display substrate itself is reduced, since only a part of the peripheral circuits is fabricated into a TFT. It also allows a more freely designed substrate having a shape and dimension according to the requirements. Further, it is possible to reduce the production cost, since the problems related to the production of the TFTs can be avoided while making those portions having a higher production yield into TFTs.

[0062]

The use of a semi-amorphous semiconductor as the semiconductor film of the TFTs enables a rapid response, making the TFTs well applicable to peripheral circuits. Thus, the TFTs for the peripheral circuits are readily fabricated simultaneously utilizing the fabrication process for the active elements without any additional special treatments.

[0063]

According to the present invention, TFTs in a complementary structure are connected to each of pixels in a matrix form, thereby a lot of advantages can be obtained as follows: (1) The threshold voltage is clear. (2) an increase of the switching speed (3) an increase of an operational margin (4) If there is a defective TFT, residual TFTs can compensate them to certain degree. (5) The number of photomasks required for manufacturing processes is increased by twice in comparison with the conventional example which uses

only NTFT. (6) The carrier mobility of the present invention is ten times or more as large as the case of using an amorphous silicon, so that the size of TFTs can be decreased with no decrease of an aperture ration in the case that two TFTs are established inside one pixel.

[0064]

Because of this, in contrast with conventional active TFT liquid crystal devices using only NTFT, the production yield can be improved and the display has vivid image.

[BRIEF DESCRIPTION OF DRAWINGS]

FIG. 1 is a liquid crystal display device according to the present invention, composed of an m X n circuit structure;

FIG. 2 is an appearance of arrangement of pixel portions in a liquid crystal display according to the present invention.

FIG. 3 shows an outline of manufacturing process of TFTs according to the present invention.

FIG. 4 shows other embodiment of the present invention.

[DESCRIPTION OF MARKS]

1, 2, . . . peripheral circuit

4 . . . IC

5 . . . peripheral circuit fabricated into TFT

6 . . . pixel

13 . . . NTFT

22 . . . PTFT

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[Procedural Amendment 1]
[Title of Document to be Amended] Specification
[Title of Item to be Amended] Brief description of drawings
[Method] Modification
[Content of Amendment]
[BRIEF DESCRIPTION OF DRAWINGS]
FIG. 1 is a liquid crystal display device according to the present invention, composed of an m X n circuit structure;
FIG. 2 is an appearance of arrangement of pixel portions in a liquid crystal display according to the present invention.
FIG. 3 shows an outline of manufacturing process of TFTs according to the present invention.
FIG. 4 shows other embodiment of the present invention.
[DESCRIPTION OF MARKS]
1, 2 . . . peripheral circuit
4 . . . IC
5 . . . peripheral circuit fabricated into TFT
6 . . . pixel
13 . . . NTFT
22 . . . PTFT

[Procedural Amendment 2]
[Title of Document to be Amended] Drawing
[Title of Item to be Amended] all drawings
[Method] Modification
[Content of Amendment]